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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,254	12/29/2000	David A. Helder	42390.P7527	8793

7590 03/11/2004

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EXAMINER	
INGBERG, TODD D	

ART UNIT	PAPER NUMBER
2124	4

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,254	HELDER ET AL.	
	Examiner	Art Unit	
	Todd Ingberg	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 26 have been examined.

Drawings

1. The drawings were received on March 12, 2001. These drawings are approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 21 are rejected under 35 U.S.C. 102(b) as being anticipated by "Parallelization of Loops With Exits On Pipelined Architectures", P. **Tirumalai** et al Hewlett-Packard Labs, 1990.

Issue of Patentable Weight

Setting a flag prior to operations and testing a flag post operation is not given patentable weight. Weather a programmer decides to presume TRUE or FALSE is not given patentable weight. This is a programming style issue and may be set by a policy in "Programming Guidelines" of the Corporation.

Claim 1

Tirumalai anticipates a method comprising: initializing to false a predicate that guards a speculative instruction in a software pipelined loop (**Tirumalai** page 201, second paragraph) ; executing at least one iteration of the software-pipelined loop (**Tirumalai** page 202, Figure 1) , including an instruction that sets the predicate to true if an associated live-in value is consumed (**Tirumalai** 205 first paragraph – dependencies is term for live-in values and page 202, dependencies) ; and executing the speculative instruction in subsequent iterations of the software pipelined loop (**Tirumalai** page 204, Table II – shows the DO loop iterations and page 205 second bullet).

Claim 2
The method of claim 1, wherein the instruction that sets the predicate true is gated by a stage predicate of the software-pipelined loop (**Tirumalai,** Figure 1).

Claim 3
The method of claim 2, wherein executing - at least one iteration of the software pipelined loop comprises executing the predicate setting instruction when the stage predicate is true. (**Tirumalai,** Figure 1).

Claim 4
The method of claim 2, wherein the stage predicate is selected to delay execution of the speculative instruction until the live-in value has been consumed. (**Tirumalai,** page 202, can be started every 19 seconds right side of page second paragraph).

Claim 5
The method of claim 1, wherein initializing to false a predicate comprises initializing to false a predicate other than a stage predicate. As per claim 1.

Claim 6
Tirumalai anticipates a method comprising: initializing a software-pipelined loop to deactivate a speculative instruction; executing at least one initiation interval (II) of the software -pipelined loop; activating the speculative instruction; and executing subsequent IIs of the software-pipelined loop. (**Tirumalai,** page 204, disabling and page 208).

Claim 7
The method of claim 6, wherein initializing the software-pipelined loop comprises initializing as false a predicate that guards the speculative instruction. As per claim 1.

Claim 8
The method of claim 7, wherein executing at least one II of the software-pipelined loop comprises executing an instruction that determines a value for the predicate guarding the speculative instruction. See the rejection for claims 1 and 3.

Claim 9
The method of claim 8, wherein activating the speculative instruction comprises executing the speculative instruction if the predicate is true. (See the rejection of claim 4 "even thou delayed it is still active).

Claim 12
The method of claim 7, wherein executing at least one II of the software-pipelined loop comprises executing an instruction that activates the speculative instruction. (**Tirumalai,** page 208, loops with multiple exits steps 1- 4)

Claim 10
The method of claim 6, wherein the speculative instruction is a compare instruction and initializing the software pipeline to deactivate the speculative instruction comprises initializing a rotating source register (**Tirumalai**, page 201, rotating register) for the compare to a value for which a predicate determined by the compare instruction is false. (**Tirumalai**, page 208, second paragraph, "with this approach ...").

Claim 11
The method of claim 10, wherein activating the speculative instruction comprises rotating a value into the source register used by the compare to determine if the predicate is true. (**Tirumalai**, page 201, rotating register)

Claim 15
The method of claim 10, wherein the inserted instruction is a compare instruction that is gated by a stage predicate. See the rejection for claim 2.

Claim 16
The method of claim 15, wherein the inserted instruction evaluates the sticky predicate as true when it is gated on by the stage predicate. See the rejection for claim 2.

Claim 17
The method of claim 16, wherein the stage predicate is selected to activate the inserted instruction once the live-in value is consumed. See the dependencies of claim 1.

Claim 13
Tirumalai anticipates a method for software pipelining a "while" loop comprising: identifying a speculative instruction in the loop; guarding the speculative instruction with a sticky predicate; initializing the sticky predicate to false; and inserting an instruction to set the sticky predicate true at a specified initiation interval of the loop. (See rejection for claim 1 and repeat of steps 1 – 4 on page 205).

Claim 14
The method of claim 13, wherein inserting an instruction comprises an instruction to set

the sticky predicate true when a live-in value targeted by the speculative instruction is consumed. As per claim 13 and dependencies of claim 1.

Claim 18

Tirumalai anticipates an apparatus comprising a machine readable medium on which are stored instructions that may be executed by a processor to implement a method comprising: executing a stage of a software-pipelined loop that includes a speculative instruction, the speculative instruction being gated off by a sticky predicate; executing an instruction that sets the sticky predicate; and executing the stage of the software -pipelined loop, including executing the speculative instruction. See the rejection for claim 1.

Claim 19

The machine-readable medium of claim 18, wherein the method further comprises initializing the sticky predicate to false to gate the speculative instruction off prior to executing the software-pipelined loop. See the rejection of claim 1 .

Claim 20

The machine-readable medium of claim 18, wherein executing an instruction that sets the sticky predicate comprises: rotating a new value (**Tirumalai**, page 201, rotating register) into a stage predicate that guards the sticky predicate setting instruction; and executing the sticky predicate setting instruction when the stage predicate is true. See rejection of claims 1 and 2

Claim 21

Tirumalai anticipates a computer system comprising: a processor to execute instructions; and a memory to store instructions which may be executed by the processor to implement a method comprising: executing an initiation interval of a software-pipelined loop that includes a speculative instruction, the speculative instruction being gated off by a sticky predicate; executing an instruction that sets the sticky predicate; and executing a subsequent initiation interval of the software-pipelined loop, including executing the speculative instruction. See the rejection for claim 1.

Claim 22

The computer system of claim 21, wherein the method further comprises initializing the sticky predicate to false to gate the speculative instruction off prior to executing the software pipelined loop. See the rejection for claim 2.

Claim 23

The computer system of claim 22, wherein executing an instruction that sets the sticky predicate comprises: rotating a new value (**Tirumalai**, page 201, rotating register) into a stage predicate that guards the sticky predicate setting instruction; and executing the sticky predicate setting instruction when the stage predicate is true.
See the rejection for claims 1 and 2.

Claim 24

Tirumalai anticipates a computer system comprising: a processor to execute instructions; and a memory to store instructions which may be executed by the processor to: initialize a software-pipelined loop to deactivate a speculative instruction; execute at least one initiation interval (II) of the software- pipelined loop; activate the speculative instruction; and execute subsequent IIs of the software-pipelined loop. (**Tirumalai**, page 205 third bullet on right, disable – see rejections for claims 1 and 2).

Claim 25
The computer system of claim 24, wherein the processor initializes the software- pipelined loop by at least initializing as false a predicate that guards the speculative instruction. See the rejection for claim 2.

Claim 26
The computer system of claim 25, wherein the processor executes at least one II of the software-pipelined loop by at least executing an instruction that determines a value for the predicate guarding the speculative instruction. See the rejection for claim 1.

Correspondence Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Todd Ingberg** whose telephone number is (703) 305-9775. The examiner can normally be reached during the following hours:

Monday	Tuesday	Wednesday	Thursday	Friday
6:15 – 1:30	6:15- 3:45	6:15 – 4:45	6:15-3:45	6:15-130

This schedule began December 1, 2003 and is subject to change.

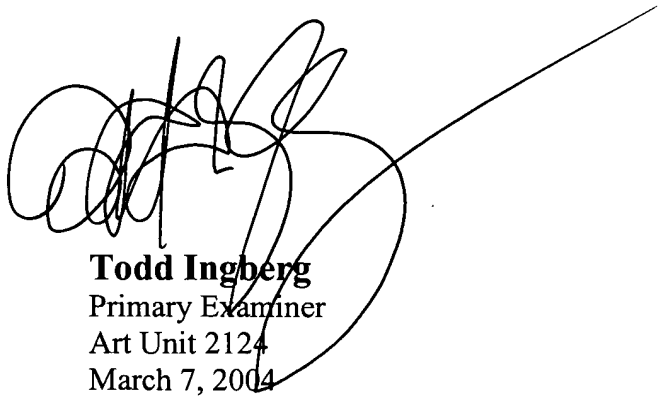
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Kakali Chaki** can be reached on (703) 305-9662. Please, note that as of August 4, 2003 the **FAX number** changed for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Also, be advised the United States Patent Office **new address** is

Post Office Box 1450

Alexandria, Virginia 22313-1450

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9700.



Todd Ingberg
Primary Examiner
Art Unit 2124
March 7, 2004